FUNCTIONAL DESCRIPTION

The Model 2365 Octal Logic Matrix is a general purpose trigger logic module which accepts 16 differential ECL inputs. These signals are applied to each of the eight independent logic channels. The outputs are differential ECL levels on a standard ECLine header. Two outputs are provided per channel. The 16-bit input size is most useful for large counter arrays, minimizing the need to cascade logic units. This results in lower cost and shorter overall trigger propagation delay.

The logic matrix for the Model 2365 is shown in Figure 1. Each channel is comprised of a series of programmable select gates which allow a wide variety of Boolean logic combinations to be assigned. These functions include:

Input Selection - Switchyard
Complementing - Input and Output
OR - Logic Fan-In
AND - Coincidence
Veto - Via Complementing Function

A CAMAC loadable test register in the Model 2365 adds to the versatility of the unit. This register may be used in diagnostics for complete CAMAC checkout of the trigger logic. The 16-bit pattern, loaded into the Test Register, may be applied to the inputs of the logic matrix by a CAMAC command. This operation simulates logic inputs for testing purposes. The eight outputs of the logic matrix may also be read via CAMAC.

The test register also allows a sophisticated veto. One requirement of the Logic Matrix is that the quiescent states of its outputs be defined by the application. For this reason, the test register is used in the veto circuit. Application of a fast front-panel ECL Veto Enable signal sets the inputs to the pattern stored in the test register for the duration of the Veto Enable pulse (≥ 10 nsec). If the quiescent input levels are loaded in the test register, proper veto operation is achieved.

SPECIFICATIONS

INPUT

Number of Inputs: 16, differential ECL DC coupled; input impedance 100 Ω, high impedance by user option, reflections < 10% for signals of ≥ 2 nsec rise time.
Minimum Input Pulse Width: 7 nsec FWHM, worst case.
Input Data Rate: DC to (> 75 MHz).
Input Connector: 17 pair front-panel header.
Veto Enable: Differential ECL input via 2-pin header. Input impedance 100 Ω, high Z by simple user modification. When asserted, the contents of the 16-bit CAMAC programmable test register are applied to the logic matrix overriding the front-panel inputs. Minimum width 7 nsec. Must precede the input by ≥ 5 nsec.

OUTPUT

Logic Outputs: Two per channel, 16 total; ECL levels, via a 34-pin header with pinouts to match the ECLine standard. Output width equals duration of logic condition.
Output Data Rate: DC to 75 MHz guaranteed.
Propagation Delay: < 10 nsec.
Analog Multiplicity: Front-panel Lemo output provides 2 mA for each logic matrix output in the logical 1 state. Rise and fall time < 4 nsec.

MEMORY PROTECTION

Continuous Memory: Memory battery backup. This feature preserves contents of memory and test register during CAMAC power down. Life of the battery is two years of operation.

MODE OF OPERATION

Data Execute: The 16 ECL input levels are applied to the octal logic matrix. Selected by the CAMAC Mode Selector bit.
Test: The contents of the 16-bit test register are applied to the logic inputs. Selected by the CAMAC Mode Selector bit.
Veto: The contents of the test register are applied to the logic inputs. Selected via front-panel Veto Enable input.

SOFTWARE SELECTED LOGIC COEFFICIENTS
(See Figure 1 and Table 1)

$A_{i,j}$: AND Selector. When set to logical 1, routes the compliment of the i^{th} input to the j^{th} logic matrix OR. When $A_{ij} = 0$, compliment unused.

$B_{i,j}$: OR Selector. When set to logical 1, routes the i^{th} input to the j^{th} logic matrix OR. When $B_{ij} = 0$ normal signal unused.

C_j: Output Complimentor. When set to logical 1, routes the compliment of the j^{th} logic matrix OR to the j^{th} output. When $C_j = 0$, the normal OR is used.

GENERAL

Packaging: In conformance with CAMAC standard for nuclear modules (ESONE Committee Report EUR4100 or IEEE Report 583. RF-shielded CAMAC #1 module.
Power Requirements: < 400 mA at +6 V; < 2.5 A at -6 V.